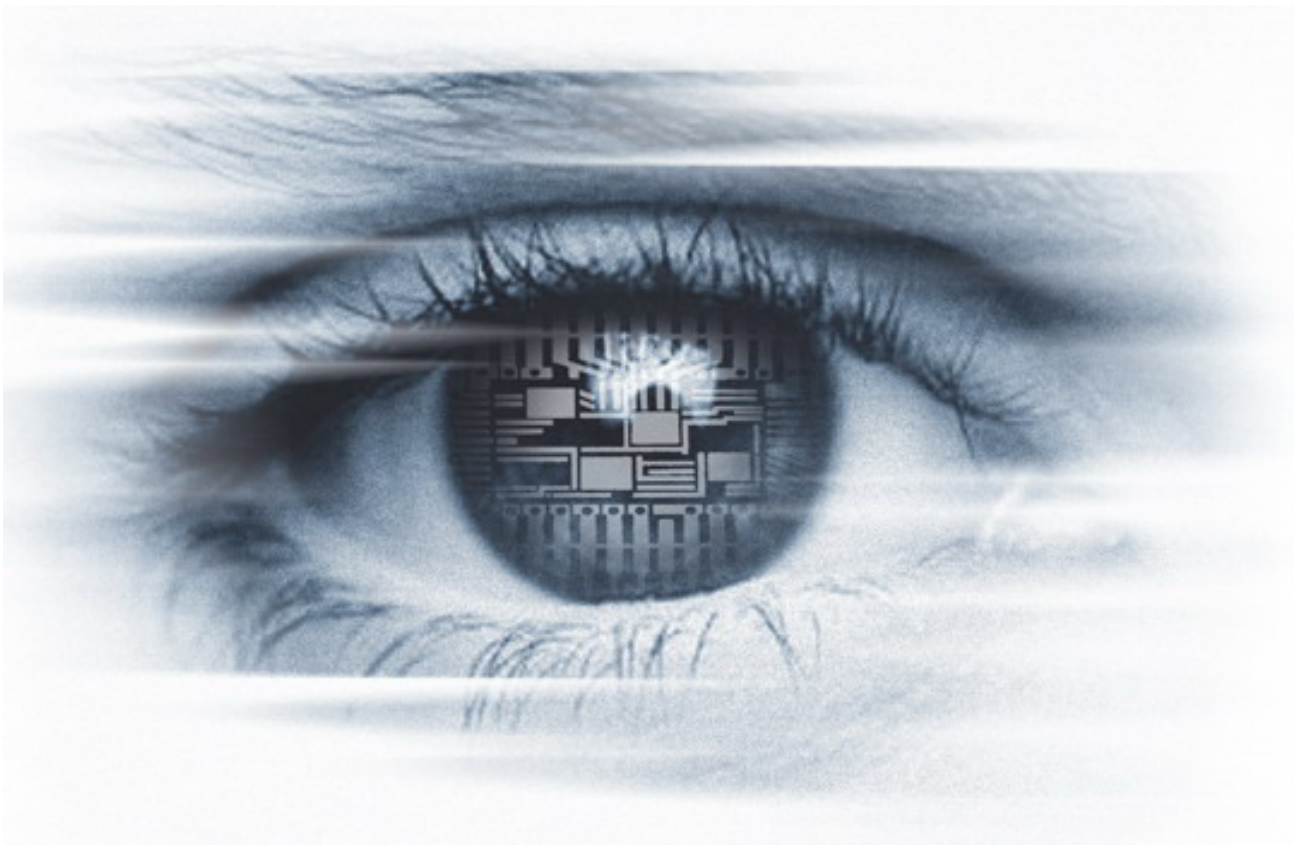
User Manual

OEM Camera Module Series

CMOS Area Scan Module Series



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1 Preface

1.1 About Photonfocus

The Swiss company Photonfocus is one of the leading specialists in the development of CMOS image sensors and corresponding industrial cameras for machine vision.

Photonfocus is dedicated to making the latest generation of CMOS technology commercially available. Active Pixel Sensor (APS) and global shutter technologies enable high speed and high dynamic range (120 dB) applications, while avoiding disadvantages like image lag, blooming and smear.

Photonfocus' product range is complemented by custom design solutions in the area of camera electronics and CMOS image sensors.

Photonfocus is ISO 9001 certified. All products are produced with the latest techniques in order to ensure the highest degree of quality.

1.2 Contact

Photonfocus AG, Bahnhofplatz 10, CH-8853 Lachen SZ, Switzerland

Sales	Phone: +41 55 451 00 00	Email: sales@photonfocus.com
Support	Phone: +41 55 451 00 00	Email: support@photonfocus.com

Table 1.1: Photonfocus Contact

1.3 Sales Offices

Photonfocus products are available through an extensive international distribution network and through our key account managers. Contacts to our key account managers can be found at www.photonfocus.com.

1.4 Further information

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1.5 Legend

In this documentation the reader's attention is drawn to the following icons:

Important note

Alerts and additional information

Attention, critical warning

Notification, user guide

2

Overview

The Photonfocus OEM camera modules contain the image sensor and all the functionality from the standard camera, except the interface and the power supply. By using the Photonfocus OEM modules the user can focus on his specific application and shorten his development time. Other than in Photonfocus cameras and board level cameras the OEM camera modules are not complete vision components. The user has to design the interface to his own electronic solution to get a complete vision solution. From this target some restrictions arise. One restriction is that Photonfocus can not guarantee the correct function of the complete solution.

Due to the open architecture of the OEM modules excessive support is often needed to implement the modules in advanced embedded solutions. Under defined boundary conditions Photonfocus provides this service on contract base. The OEM modules are not intended for the use in single volumes. The threshold in volume is from 50 modules and more per year. Long term contracts with the customer ensure the availability of the modules over a long period to predictable production dates.

For low volume projects please refer to our board level or camera products. These products are complete vision products that include the software. Due to the character of the board level and camera products Photonfocus can guarantee for the quality and functionality of these complete vision components.

The interface to the OEM modules is a 80 pin Hirose DF17 connector. The image data uses the well known AIA interface definition for vision systems (FVAL, LVAL, DVAL, DATA). Trigger inputs and strobe outputs are available. The user must supply 1.8 V, 3.3 V and 5 V.

Control of the camera settings is done with a RS232 compatible asynchronous serial interface with LVCMOS levels. There is a register based communication protocol (ASCII protocol, [MAN050]) that is suited for embedded application. Another option is to set up the software on the base of the PFRemote SDK. The Photonfocus software itself is platform independent and was already ported to different operating systems and embedded solutions.

Most OEM modules contain powerful FPGA devices and modifications in the firmware or in the software can be made on request on a contract base.

The OEM modules series that are described in this manual are listed in Table 2.1.

Name	Configuration	Description
OEM-D2048	C1	Based on the CMOSIS CMV2000 (2048x1088 pixels) and CMV4000 (2048x2048 pixels) image sensors (see Chapter 4). Monochrome, colour and NIR-enhanced models available.

Table 2.1: OEM series described in this manual (for description of configuration see Section 3.1.2)

3

Hardware Interface

3.1 Connectors

3.1.1 Power Supply

The requirements of the power supply are described in the model-specific chapter.

3.1.2 Pinout PCB connector

The pinout of the OEM camera module PCB connector is listed in the following tables (see Table 3.1, Table 3.2, Table 3.3, and Table 3.4). The signals are described in Table 3.5

Two different configurations are defined:

C1 Configuration: Image data is transmitted parallel in the AIA standard as described in 3.1.3.

C2 Configuration: Image data is transmitted in serial LVDS CameraLink® standard. This configuration supports the CameraLink® Full format.

Which configuration is used is described in the model-specific description of a module.

Pin	C1 Type	C1 Name	C2 Type	C2 Name
39	O	DATA19	I	BASE_RXN
37	O	DATA18	I	BASE_RXP
35	O	DATA17	I	PDN4
33	O	DATA16	O	BASE_TXN
31	O	DATA15	O	BASE_TXP
29	O	DATA14	I	PDN4
27	O	DATA13	O	BASE_XCN
25	O	DATA12	O	BASE_XCP
23	O	DATA11	I	PDN3
21	O	DATA10	O	BASE_X3N
19	O	DATA9	O	BASE_X3P
17	O	DATA8	I	PDN2
15	O	DATA7	O	BASE_X2N
13	O	DATA6	O	BASE_X2P
11	O	DATA5	I	PDN1
9	O	DATA4	O	BASE_X1N
7	O	DATA3	O	BASE_X1P
5	O	DATA2	I	PDN0
3	O	DATA1	O	BASE_X0N
1	O	DATA0	O	BASE_X0P

Table 3.1: Definition of the pinout of the OEM camera module PCB connector (odd row, pin 39 to 1)

Pin	C1 Type	C1 Name	C2 Type	C2 Name
79	PW	VDD_50	PW	VDD_50
77	PW	VDD_50	PW	VDD_50
75	PW	VDD_33	PW	VDD_33
73	PW	VDD_18	PW	VDD_18
71	O	DC_DC_CLK	O	DC_DC_CLK
69	O	STROBE	O	STROBE
67	I	TRIGGER	I	TRIGGER
65	I	CC2	I	PDN10
63	I	CC4	I	BASE_CC4N
61	I	CC3	I	BASE_CC4P
59	I	CC1	I	PDN9
57	O	CL_SPARE	I	BASE_CC3N
55	O	PIXEL_CLK	I	BASE_CC3P
53	O	DATA_VALID	I	PDN8
51	O	LINE_VALID	I	BASE_CC2N
49	O	FRAME_VALID	I	BASE_CC2P
47	O	DATA23	I	PDN7
45	O	DATA22	I	BASE_CC1N
43	O	DATA21	I	BASE_CC1P
41	O	DATA20	I	PDN6

Table 3.2: Definition of the pinout of the OEM camera module PCB connector (odd row, pin 79 to 41)

Pin	C1 Type	C1 Name	C2 Type	C2 Name
40	I/O	RESERVED	I/O	RESERVED
38	PW	GND	PW	GND
36	O	LED_GREEN	O	LED_GREEN
34	PW	GND	PW	GND
32	O	LED_RED	O	LED_RED
30	PW	GND	PW	GND
28	O	TCK	I	TCK
26	PW	GND	PW	GND
24	O	TMS	I	TMS
22	PW	GND	PW	GND
20	O	TDI	O	TDI
18	PW	GND	PW	GND
16	I	TDO	I	TDO
14	PW	GND	PW	GND
12	O	MISC_ANALOG	NC	RESERVED
10	PW	GND	PW	GND
8	O	MISC_DIGITAL	O	MISC_DIGITAL
6	PW	GND	PW	GND
4	O	GLOBAL_RESET	O	GLOBAL_RESET
2	PW	GND	PW	GND

Table 3.3: Definition of the pinout of the OEM camera module PCB connector (even row, pin 40 to 2)

Pin	C1 Type	C1 Name	C2 Type	C2 Name
80	PW	VDD_50	PW	VDD_50
78	PW	VDD_33	PW	VDD_33
76	PW	VDD_33	PW	VDD_33
74	PW	VDD_18	PW	VDD_18
72	PW	GND	PW	GND
70	O	TX	NC	NC
68	I	RX	NC	NC
66	PW	GND	PW	GND
64	I/O	RESERVED	I/O	RESERVED
62	I/O	RESERVED	I/O	RESERVED
60	I/O	RESERVED	I/O	RESERVED
58	I/O	RESERVED	I/O	RESERVED
56	PW	GND	PW	GND
54	I/O	RESERVED	I/O	RESERVED
52	I/O	RESERVED	I/O	RESERVED
50	I/O	RESERVED	I/O	RESERVED
48	I/O	RESERVED	I/O	RESERVED
46	PW	GND	PW	GND
44	I/O	RESERVED	I/O	RESERVED
42	PW	GND	PW	GND

Table 3.4: Definition of the pinout of the OEM camera module PCB connector (even row, pin 80 to 42)

Pins described as "reserved for future implementations" can (not a must) be connected with spare I/O signals on the customer's hardware side. All pins should be left floating (high impedance configuration) on customer's hardware side. For customer specific functionality these pins can be activated.

To enable the usage of both signal directions, please connect to I/O pins. If ever possible avoid dedicated single direction pins on FPGA's.

C1 configuration modules: For minimum configuration (such as CameraLink like interfaces) we recommend the implementation of the following signals: CC1, CC2, CC3, CC4 and CL_SPARE.

Name	Description
BASE_CC<n>N	LVDS negative, CameraLink CAMERA CONTROL BASE CC<n>
BASE_CC<n>P	LVDS positive, CameraLink CAMERA CONTROL BASE CC<n>
BASE_RXN	LVDS negative, CameraLink SERTOCAM BASE RX
BASE_RXP	LVDS positive, CameraLink SERTOCAM BASE RX
BASE_TXN	LVDS negative, CameraLink SERTOFG BASE TX
BASE_TXP	LVDS positive, CameraLink SERTOFG BASE TX
BASE_X<n>N	LVDS negative, CameraLink DATA BASE X<n>
BASE_X<n>P	LVDS positive, CameraLink DATA BASE X<n>
BASE_XCN	LVDS negative, CameraLink CLOCK BASE XC
BASE_XCP	LVDS positive, CameraLink CLOCK BASE XC
CC<n>	Trigger input, see Section 3.1.3 for additional information. (LVCMOS 3.3 V)
CL_SPARE	Reserved for future implementations
DATA<n>	Image data bit <n> (LVCMOS 3.3 V)
DATA_VALID	Data valid, indicates active data, sampled with falling PIXEL_CLK edge (LVCMOS 3.3 V)
DC_DC_CLK	DC/DC clock synchronisation pin for better noise performance. Fixed switching frequency of 1.666 MHz. We do not recommend to use this pin. It is better to reduce power supply noise with an adequate filter.
FRAME_VALID	Frame valid, indicates active frame, sampled with falling PIXEL_CLK edge (LVCMOS 3.3 V)
GLOBAL_RESET	Reset (active low) used as FPGA reset. (LVCMOS 3.3 V)
GND	Ground
LED_GREEN	Module status indicator. Indicates active image data transmission (inverted FRAME_VALID) (LVCMOS 3.3 V)
LED_RED	Module status indicator. Indicates active RS232 communication (LED_RED = RX or TX signals active) (LVCMOS 3.3 V)
LINE_VALID	Line valid, indicates active line, sampled with falling PIXEL_CLK edge (LVCMOS 3.3 V)
MISC_ANALOG	Analog voltage for customer specific purpose (0V..+5V). Not provided by all OEM camera module series.
MISC_DIGITAL	Reset (active low) used as reset for CameraLink transceiver. Compared to GLOBAL_RESET, MISC_DIGITAL is delayed and the pulse is stretched. (LVCMOS 3.3 V)
NC	Do not connect; internally used signal
PDN<n>	Input with power down in FPGA, should be grounded at interface PCB
PIXEL_CLK	Pixel clock
RESERVED	Reserved for future implementations
RX	RX RS232 interface (to camera), 3.3 V, see Section 3.1.3

Table 3.5: Signal description A-R

Name	Description
STROBE	Special strobe output. Delay, polarity and pulse width can be configured via software. (LVCMOS 3.3 V)
TCK	JTAG chain; can be routed to a customer JTAG connector
TDI	JTAG chain; can be routed to a customer JTAG connector
TDO	JTAG chain; can be routed to a customer JTAG connector
TMS	JTAG chain; can be routed to a customer JTAG connector
TRIGGER	Special trigger input. Can be configured via software. (LVCMOS 3.3 V)
TX	TX RS232 interface (from camera), 3.3 V, see Section 3.1.3
VDD_18	1.8 Volt power supply
VDD_33	3.3 Volt power supply
VDD_50	5.0 Volt power supply

Table 3.6: Signal description S-Z

3.1.3 Parallel Data Interface (C1 configuration)

The interface of the OEM camera modules in C1 configuration (see Section 3.1) is a parallel data interface, which follows the AIA standard. On the module connector the signals are available in a parallel format. The AIA standard contains signals for transferring the image data, control information and the serial communication

The user's vision system needs to be configured with the proper tap and resolution settings, otherwise the image will be distorted or not displayed with the correct aspect ratio.

Image Data Interface

The image data is transmitted by the DATA signal and by the control signals FRAME_VALID, LINE_VALID and DATA_VALID. All are sampled by the falling edge of the PIXEL_CLK signal which makes it easy to sample the signals with the rising clock edge at the receiver side.

An example timing diagram is shown in Fig. 3.1 for a 2 tap (channel) 8 bit data output. The word tap is used for parallel data channels, e.g. 2 taps means that always 2 pixels are transmitted in parallel. Not all camera modules produce an image output exactly as shown in the diagram, but the following rules are respected by all camera modules:

- All image data signals are synchronous to the PIXEL_CLK signal. All are sampled on the falling clock edge.
- An image frame starts with the rising edge of the FRAME_VALID signal and ends with the falling edge of the FRAME_VALID signal.
- An image row starts with the rising edge of the LINE_VALID signal and ends with the falling edge of the LINE_VALID signal.
- Pixel data is valid only when FRAME_VALID, LINE_VALID and DATA_VALID are asserted at the same time. It is allowed that DATA_VALID goes low during a row, as shown in Example 2 of Fig. 3.1.
- The number of pixels in a row is determined by the number of clock cycles where FRAME_VALID, LINE_VALID and DATA_VALID are asserted at the same time, multiplied by the number of taps. The number of pixels is the same in all rows of a frame.
- The time between the rising edge of the FRAME_VALID signal and the first rising edge of the LINE_VALID signal (first line pause) can be as low as 0 clock cycles. It is not required that this time is the same for all frames.
- The time between a falling edge of the LINE_VALID signal and the next rising edge of the LINE_VALID signal (line pause) can be as low as 1 clock cycle. It is not required that this time is the same for all rows.
- The time between the last falling edge of the LINE_VALID signal and the falling edge of the FRAME_VALID signal (last line pause) can be as low as 0 clock cycles. It is not required that this time is the same for all frames.

All modules that are described in this manual use either the 2 tap mode or the 3 tap mode. The data assignments for the 2 tap mode is shown in Table 3.7 and for the 3 tap mode in Table 3.8.

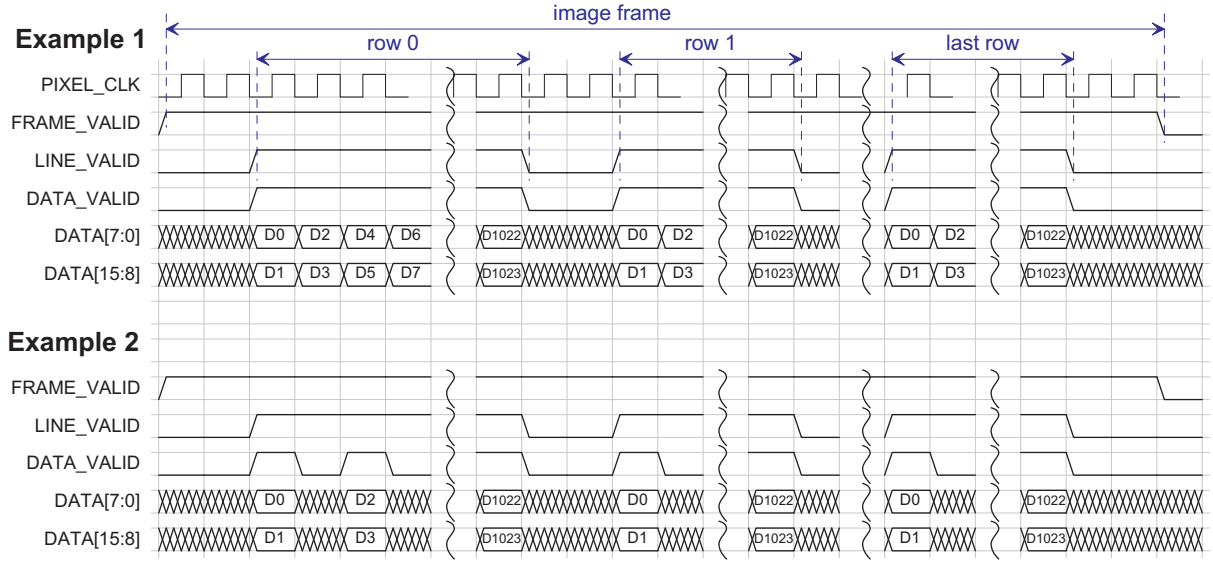

Figure 3.1: Timing examples of image data signals

Bit	Tap 0	Tap 1	Tap 0	Tap 1	Tap 0	Tap 1
	8 Bit	8 Bit	10 Bit	10 Bit	12 Bit	12 Bit
0 (LSB)	DATA[0]	DATA[8]	DATA[0]	DATA[16]	DATA[0]	DATA[16]
1	DATA[1]	DATA[9]	DATA[1]	DATA[17]	DATA[1]	DATA[17]
2	DATA[2]	DATA[10]	DATA[2]	DATA[18]	DATA[2]	DATA[18]
3	DATA[3]	DATA[11]	DATA[3]	DATA[19]	DATA[3]	DATA[19]
4	DATA[4]	DATA[12]	DATA[4]	DATA[20]	DATA[4]	DATA[20]
5	DATA[5]	DATA[13]	DATA[5]	DATA[21]	DATA[5]	DATA[21]
6	DATA[6]	DATA[14]	DATA[6]	DATA[22]	DATA[6]	DATA[22]
7 (MSB of 8 Bit)	DATA[7]	DATA[15]	DATA[7]	DATA[23]	DATA[7]	DATA[23]
8	-	-	DATA[8]	DATA[12]	DATA[8]	DATA[12]
9 (MSB of 10 Bit)	-	-	DATA[9]	DATA[13]	DATA[9]	DATA[13]
10	-	-	-	-	DATA[10]	DATA[14]
11 (MSB of 12 Bit)	-	-	-	-	DATA[11]	DATA[15]

Table 3.7: 2 Tap data assignment

Bit	Tap 0	Tap 1	Tap 2
0 (LSB)	DATA[0]	DATA[8]	DATA[16]
1	DATA[1]	DATA[9]	DATA[17]
2	DATA[2]	DATA[10]	DATA[18]
3	DATA[3]	DATA[11]	DATA[19]
4	DATA[4]	DATA[12]	DATA[20]
5	DATA[5]	DATA[13]	DATA[21]
6	DATA[6]	DATA[14]	DATA[22]
7	DATA[7]	DATA[15]	DATA[23]

Table 3.8: 3 Tap data assignments

Trigger

Various trigger input signals are available. The naming used in the CameraLink manual and in the GigE manual is slightly different, see Table 3.9. Some trigger signals are not available on all camera module models, see the manual of the underlying standard camera for more information.

Signal Name	CL Name	GigE Name	Notes
TRIGGER	I/O Trigger	Line 1 Trigger	This signal is inverted in the FPGA
CC1	Interface Trigger	PLC_Q4	
CC2	CC2	PLC_Q5	
CC3	CC3	PLC_Q6	
CC4	CC4	PLC_Q7	

Table 3.9: Naming of the trigger signals

Serial Configuration

The OEM camera modules can be controlled by the user via a RS232 compatible asynchronous serial interface with LVCMOS levels (signals TX and RX). The interface is accessible via the board connectors.

The preferred method to control the camera through the serial interface is with the ASCII protocol that is described in [MAN050].

Another option is to set the software on the base of the PFRemote SDK. The Photonfocus software itself is platform independent and was already ported to different operating systems and embedded solutions. The compiled PFRemote (pflib) SDK can be downloaded from the Photonfocus web page www.photonfocus.com.

3.1.4 Module Connector

The PCB board-to-board connectors (DF17 series, two-piece connector, stacking height 5-8 mm) are available from Hirose (www.hirose-connectors.com). Details of the order numbers are listed in Table 3.10.

Connector type	Part Number	virtual height	location
Header	DF17(2.0)-80DP-0.5V	2 mm	Processing board (Photonfocus side)
Receptacle	DF17(4.0)-80DS-0.5V	4 mm	Processing board (customer side)
Receptacle	DF17(3.0)-80DS-0.5V	3 mm	Processing board (customer side)

Table 3.10: Ordering details of the PCB board-to-board connectors (HRS connectors)

☞ All parts on the PCB boards implemented by Photonfocus are $\leq$ 3mm.

Please check for the overall mounting height of the PCB board-to-board connector (see Fig. 3.2). The choice of a 5 mm receptacle may result in part collision.

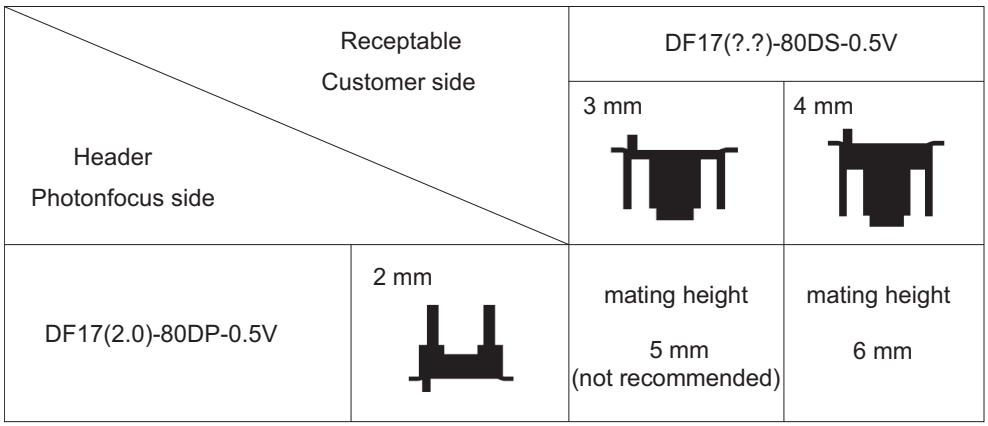

Figure 3.2: Mating height of the header and receptacle of the PCB board-to-board connectors (Hirose connectors)

4

OEM-D2048

4.1 Overview

The Photonfocus OEM-D2048 imaging modules series is built around the CMOS image sensors CMV2000 and CMV4000 from CMOSIS, that provide a resolution of 2048 x 1088 (CMV2000) or 2048 x 2048 pixels (CMV4000). The module series is optimized for low light conditions and there are standard monochrome, NIR enhanced monochrome (I) and colour (C) models. The modules are aimed at standard applications in industrial image processing where high sensitivity and high frame rates are required.

4.2 OEM-D2048 Naming Convention

The naming convention of the OEM-D2048 camera series is summarized in Fig. 4.1.

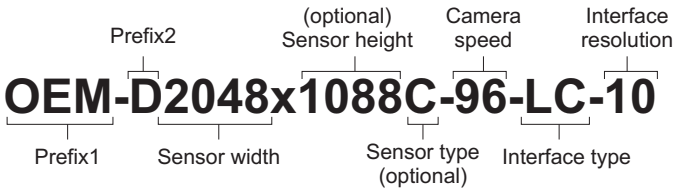

Figure 4.1: Camera naming convention

Prefix1 `OEM` is currently the only used Prefix1.

Prefix2 Camera family specifier. The following specifiers are used in this manual: `"D"`: standard area scan cameras; `"L"`: cameras with dedicated line scan mode

Sensor width All cameras covered in this chapter use sensors with a width of 2048 pixels.

Sensor height This indication is optional to avoid ambiguity. The modules that use the 2 MPix CMV2000 sensor have a height indicator of `"1088"`. The modules that use the 4 MPix CMV4000 sensor don't have a height indication. The exception are the L-models (Prefix2='L') that have a CMV2000 image sensor.

Sensor type Available sensor types are: `"I"`: NIR enhanced sensors, `"C"`: colour cameras. Cameras without sensor type specifier have a standard monochrome sensor.

Camera speed The camera speed is usually the product of the camera interface clock in MHz and the number of parallel interface channels (taps).

Interface type All modules covered by this chapter have a Low Power CMOS (LVCMOS) interface denoted by `"LC"`.

Interface resolution Maximal resolution (bit width) of the camera interface.

4.3 Available Models

Table 4.1 and Table 4.2 show lists of available OEM modules with the CMOSIS CMV2000 or CMV4000 image sensors. These modules have the firmware of a corresponding standard camera which is shown in the list. The specification of the functionality is shown in the chapter "Functionality" of the corresponding manual: for CL interface refer to [MAN054] and for G2 interface refer to [MAN055]. The interface is not included in the OEM modules.

All available models use C1 configuration (parallel data interface) (see also Section 3.1.2).

Name	Sensor	Taps	Clock	Standard Camera
OEM-D2048x1088-160-LC-10	2MP Mono	2	80 MHz	MV1-D2048x1088-160-CL-10
OEM-D2048x1088I-160-LC-10	2MP NIR	2	80 MHz	MV1-D2048x1088I-160-CL-10
OEM-D2048x1088C-160-LC-10	2MP Color	2	80 MHz	MV1-D2048x1088C-160-CL-10
OEM-D2048x1088-240-LC-8	2MP Mono	3	80 MHz	MV1-D2048x1088-240-CL-8
OEM-D2048x1088I-240-LC-8	2MP NIR	3	80 MHz	MV1-D2048x1088I-240-CL-8
OEM-D2048x1088C-240-LC-8	2MP Color	3	80 MHz	MV1-D2048x1088C-240-CL-8
OEM-D2048-160-LC-10	4MP Mono	2	80 MHz	MV1-D2048-160-CL-10
OEM-D2048I-160-LC-10	4MP NIR	2	80 MHz	MV1-D2048I-160-CL-10
OEM-D2048C-160-LC-10	4MP Color	2	80 MHz	MV1-D2048C-160-CL-10
OEM-D2048-240-LC-8	4MP Mono	3	80 MHz	MV1-D2048-240-CL-8
OEM-D2048I-240-LC-8	4MP NIR	3	80 MHz	MV1-D2048I-240-CL-8
OEM-D2048C-240-LC-8	4MP Color	3	80 MHz	MV1-D2048C-240-CL-8
OEM-L2048-160-LC-10	2MP Mono	2	80 MHz	MV1-L2048-160-CL-10
OEM-L2048I-160-LC-10	2MP NIR	2	80 MHz	MV1-L2048I-160-CL-10
OEM-L2048C-160-LC-10	2MP Color	2	80 MHz	MV1-L2048C-160-CL-10

Table 4.1: Available Models OEM-D2048 based on CameraLink standard cameras

Name	Sensor	Taps	Clock	Standard Camera
OEM-D2048x1088-80-LC-10	2MP Mono	2	40 MHz	MV1-D2048x1088-80-G2-10
OEM-D2048x1088I-80-LC-10	2MP NIR	2	40 MHz	MV1-D2048x1088I-80-G2-10
OEM-D2048x1088C-80-LC-10	2MP Color	2	40 MHz	MV1-D2048x1088C-80-G2-10
OEM-D2048x1088-96-LC-10	2MP Mono	2	48 MHz	MV1-D2048x1088-96-G2-10
OEM-D2048x1088I-96-LC-10	2MP NIR	2	48 MHz	MV1-D2048x1088I-96-G2-10
OEM-D2048x1088C-96-LC-10	2MP Color	2	48 MHz	MV1-D2048x1088C-96-G2-10
OEM-D2048-96-LC-10	4MP Mono	2	48 MHz	MV1-D2048-96-G2-10
OEM-D2048I-96-LC-10	4MP NIR	2	48 MHz	MV1-D2048-96I-G2-10
OEM-D2048C-96-LC-10	4MP Color	2	48 MHz	MV1-D2048C-96-G2-10
OEM-L2048-96-LC-10	2MP Mono	2	48 MHz	MV1-L2048-96-G2-10
OEM-L2048I-96-LC-10	2MP NIR	2	48 MHz	MV1-L2048I-96-G2-10
OEM-L2048C-96-LC-10	2MP Color	2	48 MHz	MV1-L2048C-96-G2-10

Table 4.2: Available Models OEM-D2048 based on GigE standard cameras

4.4 Mechanical Interface

During storage and transport, the camera modules should be protected against vibration, shock, moisture and dust. The original packaging protects the camera modules adequately from vibration and shock during storage and transport. Please either retain this packaging for possible later use or dispose of the packaging according to local regulations.

The OEM-D2048 camera module consists of two PCB: the sensor PCB and the Processing PCB. Overviews of the two boards are shown in Fig. 4.2 and Fig. 4.3.

The front side of the Sensor PCB has a copper border. The customer housing should be designed to contact with this copper border for proper heat dissipation.

Several temperature monitors are integrated on the camera modules to supervise system reliability.

STEP files of the OEM camera modules are available on request.

During development phase, the temperature monitors can be used to check whether the customers housing sufficiently supports the heat sink.

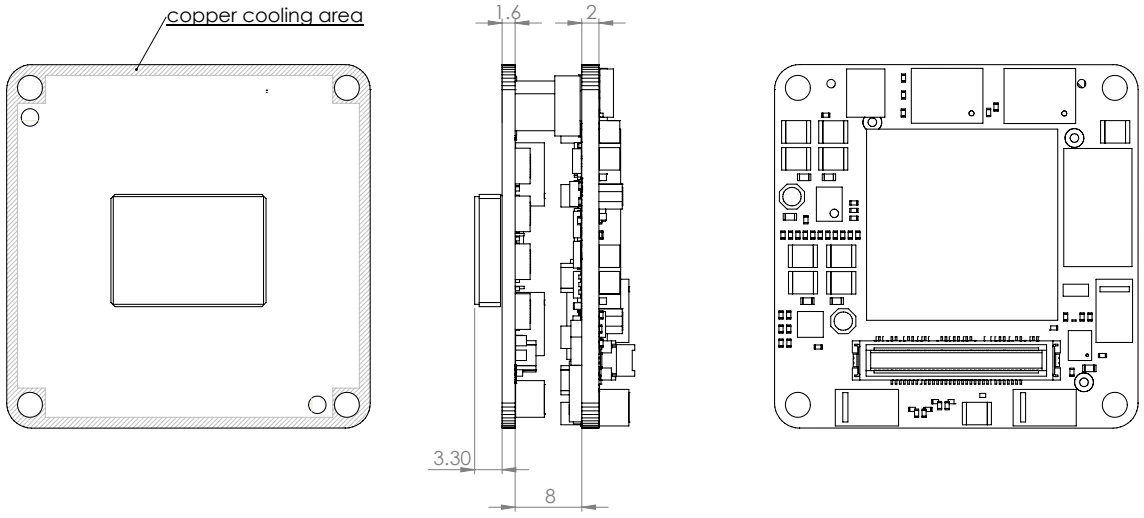

Figure 4.2: Mechanical overview of OEM-D2048 modules; left: Sensor PCB, middle: PCB connected, right: Processing PCB

4.4.1 OEM-D2048 Sensor PCB

Fig. 4.4 shows the dimensions of the OEM-D2048 Sensor PCB equipped with the CMV2000 (2 MP) sensor and Fig. 4.5 equipped with the CMV4000 (4 MP) sensor.

An outline of the CMV2000 image sensor is shown in Fig. 4.6 and of the CMV4000 in Fig. 4.7.

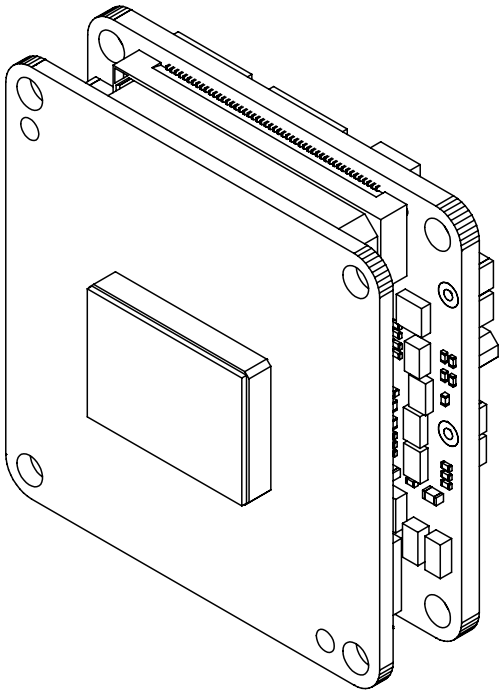

Figure 4.3: OEM-D2048 modules side view

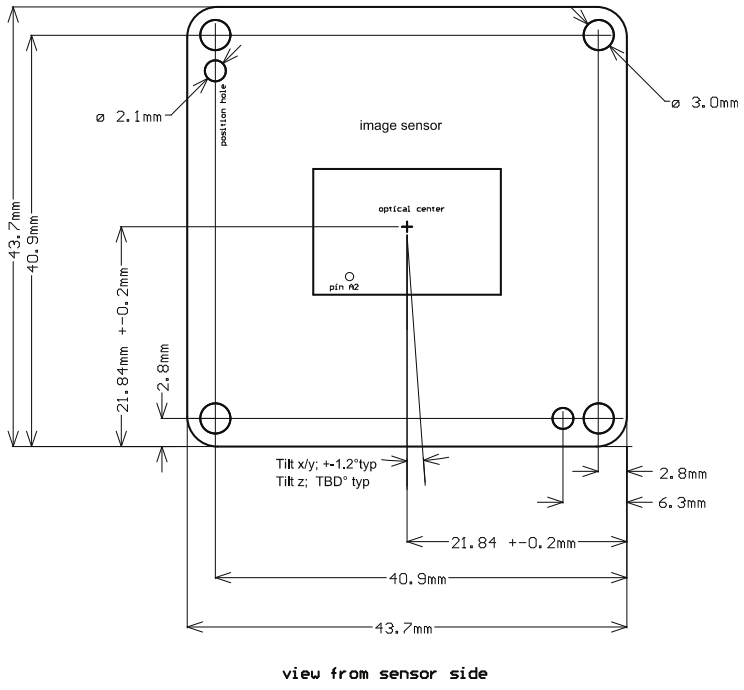

Figure 4.4: Dimensions of the OEM-D2048 Sensor PCB with CMV2000 (2 MP) sensor

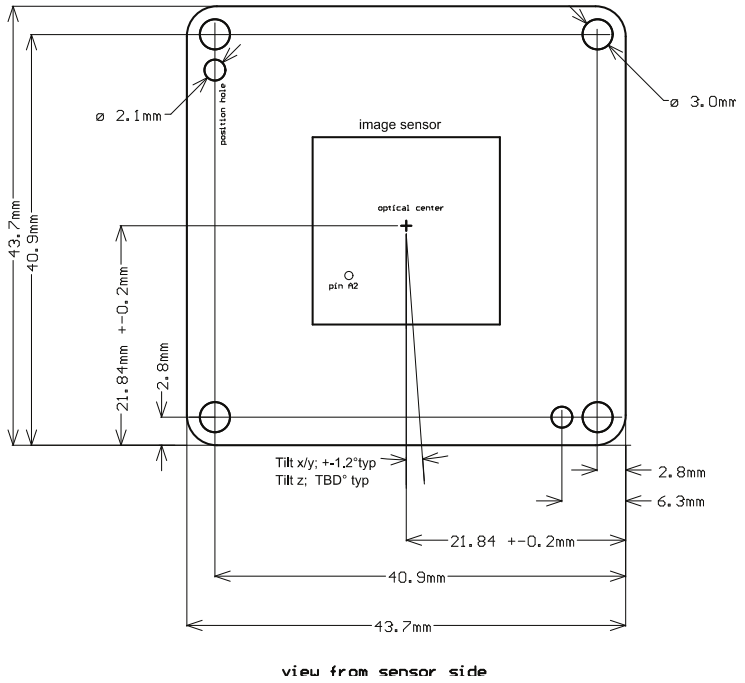

Figure 4.5: Dimensions of the OEM-D2048 Sensor PCB with CMV4000 (4 MP) sensor

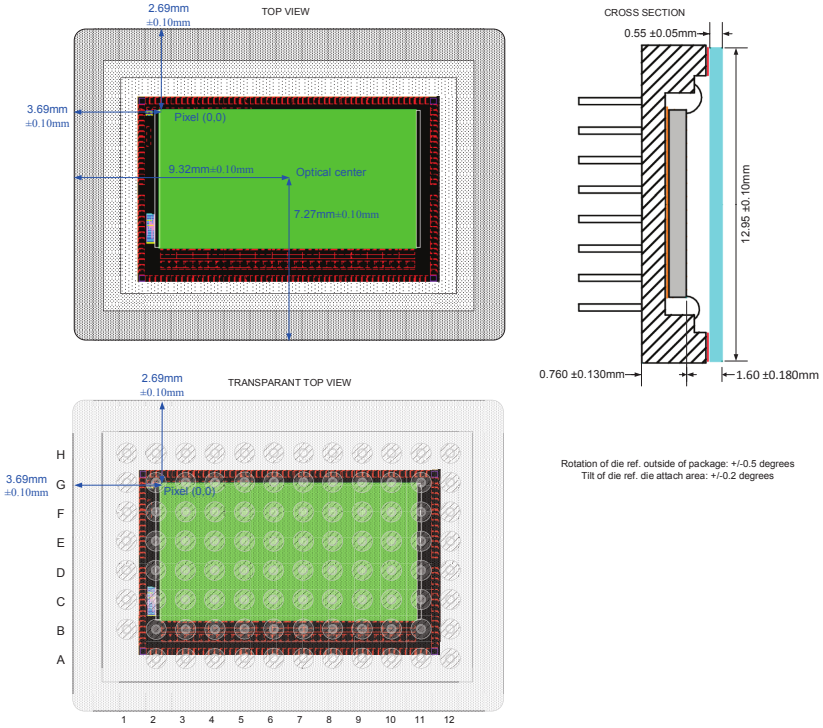

Figure 4.6: Outline of the CMV2000 (2 MP) sensor

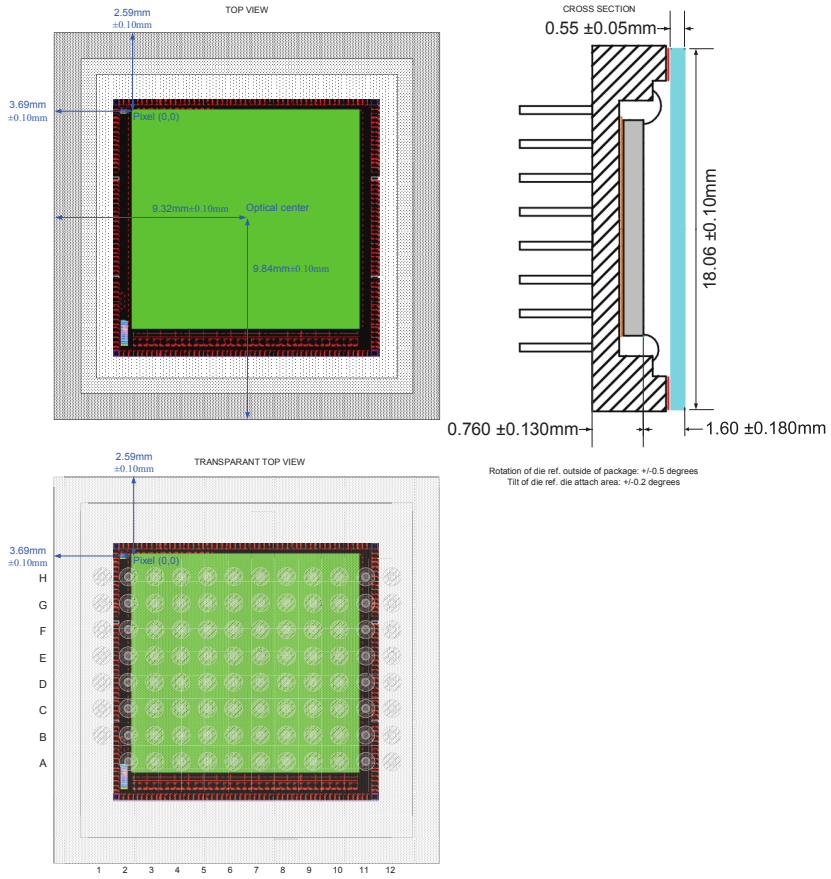

Figure 4.7: Outline of the CMV4000 (4 MP) sensor

4.4.2 OEM-D2048 Processing PCB

Fig. 4.8 shows the dimensions of the OEM-D2048 Processing PCB.

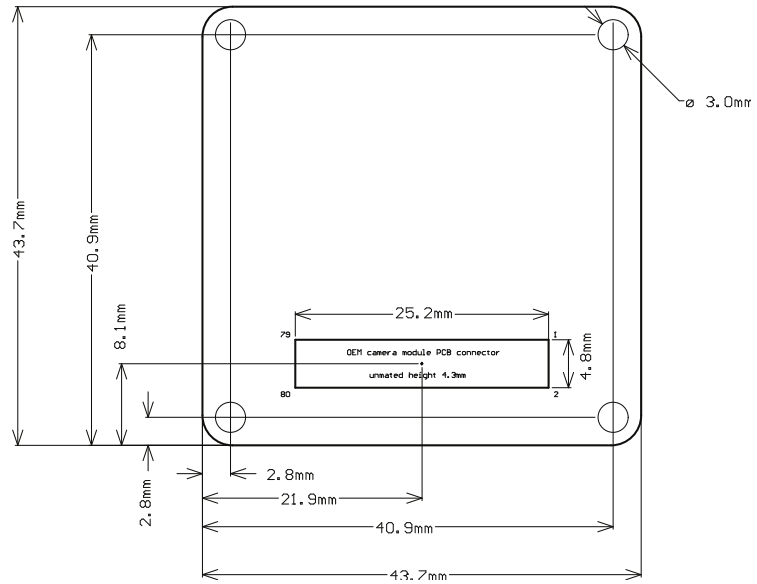

Figure 4.8: Dimensions of OEM-D2048 Processing PCB

4.5 Power Supply

The OEM camera modules require three power supply voltages. The OEM camera modules meet all performance specifications using standard switching power supplies, although well-regulated linear power supplies provide optimum performance.

It is extremely important that you apply the appropriate voltages to your OEM camera module. Incorrect voltages will damage the OEM camera modules.

Table 4.3 summarizes the specifications for the power supply voltages and Table 4.4 summarizes the specifications for the supply current.

The maximum noise level should not exceed +/- 20 mV

Parameter	Symbol	MIN	TYP*	MAX
Supply Voltage	VDD_18	1.764 V	1.8 V	1.836 V
Supply Voltage	VDD_33	3.234 V	3.3 V	3.366 V
Supply Voltage	VDD_50	4.900 V	5.0 V	5.100 V
Supply Voltage	P_V	-	2.88 W	-

Table 4.3: Electrical characteristics of the OEM-D2048 camera module (Indicated values are typical values at 25 °C)*

Parameter	Symbol	MIN	TYP*	MAX
Supply Current	IDD_18	-	0 mA	0 mA
Supply Current	IDD_33	-	102 mA	2080 mA
Supply Current	IDD_50	-	500 mA	820 mA

Table 4.4: Electrical characteristics of the OEM-D2048 camera module (Indicated values are typical values at 25 °C*

5 Warranty

The manufacturer alone reserves the right to recognize warranty claims.

5.1 Warranty Terms

The manufacturer warrants to distributor and end customer that for a period of two years from the date of the shipment from manufacturer or distributor to end customer (the "Warranty Period") that:

- the product will substantially conform to the specifications set forth in the applicable documentation published by the manufacturer and accompanying said product, and
- the product shall be free from defects in materials and workmanship under normal use.

The distributor shall not make or pass on to any party any warranty or representation on behalf of the manufacturer other than or inconsistent with the above limited warranty set.

5.2 Warranty Claim

The above warranty does not apply to any product that has been modified or altered by any party other than manufacturer, or for any defects caused by any use of the product in a manner for which it was not designed, or by the negligence of any party other than manufacturer.

6

References

All referenced documents can be downloaded from our website at www.photonfocus.com.

SW002 PFLib Documentation, Photonfocus, August 2005

AN010 Application Note "Camera Clock Concepts", Photonfocus, July 2004

AN026 Application Note "LFSR Test Images", Photonfocus, September 2005

MAN050 User Manual "Register based ASCII Protocol", Doc-ID MAN050

MAN054 User Manual "Photonfocus D/L-2048 CameraLink® Series", Doc-ID MAN054

MAN055 User Manual "Photonfocus D/L-2048 Gigabit Ethernet Series", Doc-ID MAN055

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Revision History

Revision	Date	Changes
1.0	September 2013	First release
1.1	November 2014	OEM-D2048: Missing values in electrical characteristics added